Abstract

Ceramic and laminate multilayered technologies are explored in the design of novel circuit topologies and in novel implementations of classical circuit topologies. A cross-slot coupled filter topology implemented in folded substrate integrated waveguide (FSIW) is proposed and is shown to exhibit properties that make it favourable for diplexer design. A C-Band diplexer design is presented. The diplexer is fabricated in both Liquid crystalline Polymer (LCP) and Printed Circuit Board (PCB) multilayed technology. The viability of both processes for this type of circuit is analysed and performance is verified by simulation and measurement. A 'ridge-like' folded substrate integrated waveguide resonator is proposed. A comparative analysis of this resonator and a traditional ridge waveguide resonator structure in substrate integrated technology is presented. For rectangular waveguide resonators with identical outer dimensions, the former is shown to achieve lower operational frequencies relative to the latter. Two X-band filters are designed using the 'ridge-like' FSIW resonator. Both filters are fabricated in PCB multilayered technology and performance is verified by both simulation and measurement. The measurement results of the first, a second order filter, show a maximum insertion loss of 2.23 dB for the primary band and a wide frequency range of 7.5 GHz between the first passband and the second. The second filter is a fourth order filter which achieves a maximum measured insertion loss of 4.7 dB for the primary passband with the second passband occuring over 8.5 GHz away. A classical sequence asymmetric RC polyphase filter (PPF) is implemented in low temperature co-fired ceramics (LTCC) technology. The novel implementation realises a miniaturised structure comprising embedded components interconnected using planar transmission lines. Verification of the structure's performance is by simulation of a three segment PPF. The LTCC PPF is shown to achieve an image suppression of 35 dB over a frequency range of 100 MHz to 300 MHz and a gain error of 0.14dB between its quadrature outputs. The final design is a novel implementation of a miniaturised two-stage PIN Diode limiter-switch in LTCC. The structure comprises both embedded components and surface mount components interconnected using planar transmission lines and vias. Circuit viability is assessed through simulation of a multilayered L-Band limiter-switch design. An insertion loss of 0.25 dB and a return loss of 25.34 dB at a center frequency of 1.3 GHz are obtained when the switch is in its off-state. When a large 1 ms input pulse signal of 45 dBm is applied at the input of the limiter-switch, the resulting output pulse has a flat leakage of approximately 16.4 dBm.