Comparative Study of Potential Induced Degradation Approaches in Multi-crystalline Si PV Modules

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Abstract

Potential Induced Degradation (PID) causes major reliability issues, since it results in significant performance degradation and negatively affects the durability of cells, modules and PV systems. In this work three methods are used to induce PID on three modules (A, B and C) by applying a voltage of 1000V to the frame, an aluminium sheet and a plate respectively. In the first method the voltage is applied to the aluminium frame while the temperature is kept at 35 °C ± 1°C and humidity levels at 70% RH ± 5% RH. In the second method, an aluminum sheet covers the glass surface without touching the frame and acts as a positive terminal connection, temperature of 35 ºC ± 1 ºC and humidity of below 40%RH. The third method, involves a smaller aluminium plate which only covers one cell under the same environmental conditions as for method 2. The extent of degradation is determined by measuring the maximum power before and after the PID stress and using Electroluminescence (EL) Imaging taken at a current corresponding to 10% of Isc. The power dropped by 29.6% in 288 hours, 88.7% in 48.0 hours and 6.2% in 96.0 hours in the three separate methods respectively. This study showed that certain modules may not be easily susceptible to PID, unless subjected to a high system voltage over a long period of time such as modules deployed over a long period of time in the field.

Keywords: PID; Reliability; System Voltage; Electroluminescence

1. Introduction

Photovoltaic (PV) modules are deployed in the field where they are subjected to high temperatures and high humidity levels. Over a long period of time moisture may ingress through the back sheet, on reaching the glass/encapsulation interface the moisture may dissolve soda lime within the glass creating free sodium ions making the module highly susceptible to PID. The susceptibility of a module to PID may depend on the thickness of the cells' anti-reflective coating and manufacturing crystal defects, resistivity of the module encapsulation, exposure to voltage stress and environmental conditions (temperature and humidity)[1][2][3][4]. New modules are ordinarily free from sodium ions and hence can be termed as PID free. The conditions causing PID in the field can be replicated in the lab by subjecting the module to a high potential between the cover glass (via the frame, aluminium sheet or plate) and the cell circuit and increased temperature and humidity conditions subject to standard IEC-TS-62804-1:2015 [5]. The high potential difference between the module's earthing via the glass and the active circuit creates a strong electric field which causes a small leakage current to develop between the glass and cells. The leakage current may increase when sodium ions are caused to drift towards the cell surface resulting in heavy shunting[6]. The main objective of this work is to induce PID on crystalline modules using three different methods and compare power degradation rates on new and deployed PV modules.

2. Theory

2.1. Modelling current leakage paths

Most PV power plants are constructed using a transformerless configuration, hence the grid and PV power plant string circuits may not be isolated[7]. Since there is no guarantee of isolation, a high potential of several hundred volts may develop between the earthing and the module active circuit in such strings, resulting in a small leakage current to flow between the module active circuit and the frame (ground). The size of the leakage current may increase with availability of sodium ions which may migrate towards the cells and eventually at the right concentration may diffuse into the PN junction resulting in high shunting and increased electron-hole recombination sites.

Figure 1 shows a schematic illustration of a PV module structure and the possible leakage current paths in a p-type module. These leakage paths are: 1) along the glass surface, 2) through the glass substrate, 3) through the interface between glass and the encapsulation, 4) through the encapsulation substrate, 5) through the interface between the back encapsulation and the back sheet, 6) through the back sheet and 7) along the back sheet surface[6]. The use of encapsulation materials with high resistivity may minimize sodium ion migration from glass to the cell surface

hence lowering PID shunting [8].

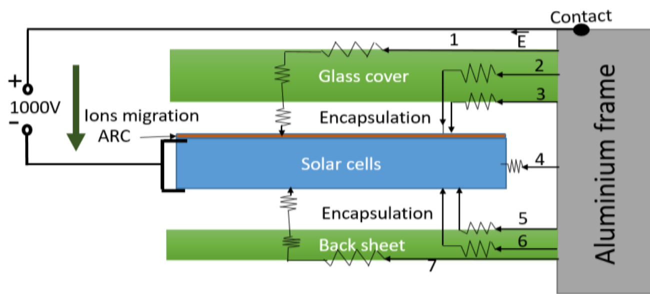


Fig. 1. A cross section of mc-Si PV module constructed to indicate current modelled current leakage: 1) along the glass surface, 2) through the glass substrate, 3) through the interface between glass and the encapsulation, 4) through the encapsulation substrate, 5) through the interface between the back encapsulation and the back sheet, 6) through the back sheet and 7) along the back sheet surface

2.2. Electroluminescence (EL) imaging

EL imaging is a non-destructive technique that is used to detect module degradation including PID. The intensity of the emitted luminescence is proportional to the number of minority charge carriers going into the cell [4]. The EL setup consists of a CCD camera and a power supply which is connected in forward bias. The biasing drives current to the module to the short-circuit current (Isc) of the module and 10% of Isc. In an EL image of an ideal module (with no damage or degradation) all the cells have relatively uniform intensity and brightness. PID affected modules will causes cells to appear at varied degree of darkness 'checkerboard pattern'. The decreased intensity is due to increased shunting resulting in increased recombination sites and leakage current paths. This effect is visible at low current EL (10% Isc) because minority charge carriers in the shunted cells undergo non- radiative recombination, emitting a lower intensity EL signal.

2.3. *Power measurements*

The Current-Voltage (I-V) measurements of modules are taken at STC (temperature 25°C, irradiance of 1000 W/m^2 and AM 1.5) using an indoor solar simulator. PID affected modules have decreased shunt resistance which results in decreased maximum power (MMP), Fill Factor (FF), and Open-circuit voltage (Voc). The decreased shunt resistance causes the slope of the curve in the short circuit (Isc) region to decrease and the FF which is a measure of the 'squareness' of the curves to decreases. The PID affected cells experience shunting that creates parallel current paths. This increased leakage current leads to a drop in the module efficiency, which is calculated as the ratio of power output to power input [9].

3. Experimental

3.1. Modules

In this study three 60-cell multi-crystalline modules with dimensions 1960mm × 990mm × 35mm were subjected to three different PID stress methods. The modules are commercially available p-type modules. Module A was a new module classified as PID resistant by the manufacturer. Module B and module C had been deployed for more than five years and were not specifically classified as PID resistant.

Module	Initial MPP (W)	PID Induction Method	Classified as PID resistant by Manufacturer
A	265.9	Method 1 - 288 hrs	Yes
B	233.9	Method 2 – 48 hrs	No
C	229.5	Method 3 – 96 hrs	No

Table 1. Module specifications

3.2 PID stress methods

EL images and power measurements were taken for each module before and after PID stress. The three PID stress methods used in this study involve using a breakdown voltage and insulation resistance (HiPot) analyser to establish a strong electric field at various points in the module. The methods are explained in the sections below.

3.2.1 Method 1: PID induction using an environmental chamber

The module is connected such that the frame is positively biased while the module terminals are short circuited and connected to the negative terminal of the safety analyser. The safety analyser monitors the leakage current and maintains a voltage of 1000 V for a cycle of 96 hours. To reduce the electrical resistance of the module cover glass, the module is placed inside an environmental chamber which is set at 35 °C ± 1 °C and humidity levels of 70 ± 5% RH. The environmental chamber used was constructed to specifically meet the needs for this project as a cost effective alternative to expensive commercially available chambers.

3.2.2 Method 2: PID induction using an aluminium sheet covering the surface

In this method, an aluminium sheet (1625mm x 955mm x 3mm)

is laid on the module cover glass without making contact with the module frame. The aluminium sheet provides a conductive path on the glass surface simulating high humidity conditions. The aluminium sheet was connected to the positive terminal while the module terminals were short circuited and connected to the negative terminal of the voltage safety analyser which supplied 1000V for 48 hours. The temperature was kept at 35 °C ± 1 °C while humidity is maintained at below 40 %RH.

In method 2, a strong electric field in figure 2 is responsible for the drift of sodium ions to the surface of the cells and diffusion into the PN junction resulting in heavy shunting. This confirms that even a frameless module would still degrade under high voltage stress, provided the module has free sodium ions and the cover glass material is of low electrical resistivity.

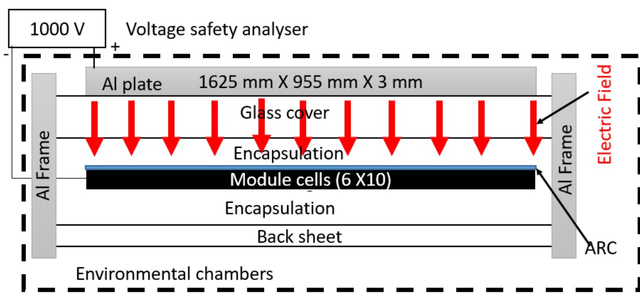


Fig. 2. PID induction experimental set up: Method 2 - the anode is connected to an aluminium the plate size of the module not touch the frame; the red lines indicate the electric field between the aluminium plate and the module cells, ARC (Anti-reflecting coating)

3.2.3 Method 3: A localised PID induction

An aluminium plate measuring 157 mm × 157 mm × 3 mm approximating the area of a cell was placed over a single module cell. The plate was positively biased while the short-circuited module terminals are biased to the negative of the safety analyser which supplies 1000V for 96 hours. The temperature was maintained at 35 °C ± 1 °C while humidity maintained at below 40 %RH. Similar to Method 2, this method simulates a conductive glass surface, but in a smaller area of the module. This method can be used to investigate the role of current paths in PID induction.

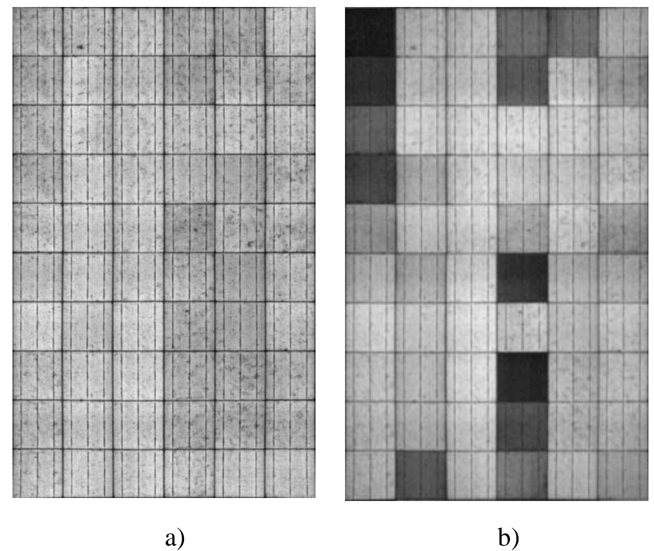
4. Results and discussion

4.1. Method 1

Module A was subjected to PID stress using method 1. The initial EL image (10%Isc) showed uniform brightness across the cells except areas with manufacturing defects (dark spots) and grain boundaries, figure 3(a). After PID stress, the EL images taken at a current corresponding to 10% of Isc showed several cells which are significantly darker than the other cells in the module, figure 3(b). Parallel shunt current paths have formed in these cells due to PID. The majority of the affected cells are next to the frame. This pattern around the frame is commonly observed in PID affected modules in the field and in those tested in an environmental chamber at higher temperature conditions according to IEC-62804-1[6]. The electric field closer to the frame may be bigger due to the lower resistance from the conductive moisture on the cover glass close to the positively biased frame[10].

The initial and final power measurements for module A are given in table 2. After 3 cycles of 96 hours, totalling 288 hours the power of the module had degraded by 29.6%. The Fill Factor of the curve also decreased indicating the increased shunting paths in the module.

This method is closer to the conditions that are experienced in the field. After subjecting the module to a high voltage and high humidity for an extended test period (3 cycles), even this module that is categorised as PID resistant, degraded.



a) b)

Fig. 3. Module A, EL images taken at 10% of Isc (0.982A), a) Initial EL image, b) EL image after 288 hours of PID stress.

Module	**PID**	**V_{oc}**	**P_{max}**	**FF**	**Efficiency**	**Dg Rate (W/h)**
A	Before	37.9	265.9	0.77	13.71	0.27
	After	36.6	187.1	0.60	9.64	
	% Dg	**-0.03**	**-29.6**	**-22**	-30	

B	Before	36.7	230.2	0.76	11.86	4.25
	After	13.4	26.1	0.27	1.33	
	% Dg	**-63.5**	**-88.7**	**-64**	**-89**	
C	Before	36.6	234.8	0.77	12.10	0.15
	After	36.3	220.3	0.73	11.35	
	% Dg	**-0.8**	**-6.2**	**-5.0**	**-6.0**	

Table. 2. Module power measurements summary. *Dg is Degradation

4.2. Method 2

Module B, which had been previously deployed, was subjected to PID stress using method 2. The EL images were taken before and after PID stress at a current corresponding to 10% Isc as shown in figure 4a and figure 4b respectively. The EL image taken after PID stress appears completely dark, indicating that all of the cells have been severely shunted.

After 48 hours of PID stress the module had lost 88.7% of the initial power output, while Voc and FF of the module decreases considerably by 63.5% and 64.0% respectively, table 2. The rate of degradation is considerably higher than method 1 since the Al sheet acts as a conductive layer over the entire cover glass, equivalent to stress the module at very high humidity levels.

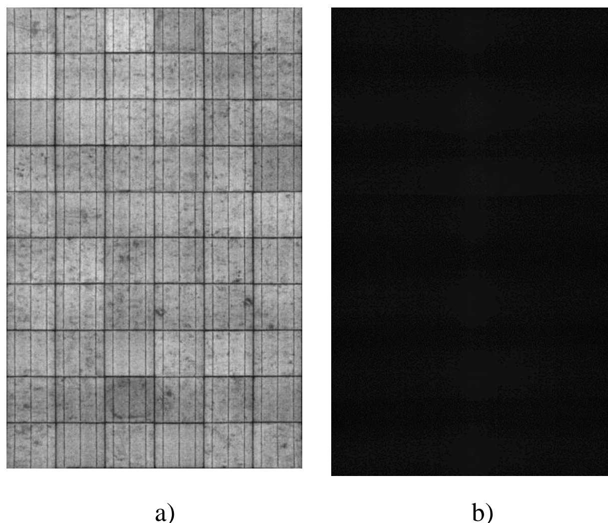


Fig. 4. Module A, EL images taken at 10% of Isc (0.982A), a) Initial EL image, b) EL image after 48 hours of PID stress.

4.3. Method 3

For method 3, localised PID stress was induced using an Al plate placed on a single cell (cell position C6 blue shaded) as indicated on module C, figure 5a. The EL images were taken before and after PID stress at a current corresponding to 10% of Isc as shown in figure 5a and figure 5b respectively. After the 96 hours of PID stress, shunting is observed in cell C6 and the neighbouring cells (C5, C7, B6 & E6) and also other cells not in the neighbourhood of the cell of interest (C10 & D10). This result shows that the glass must be conductive and affects the formation of leakage current paths in other part of the module. Further study is needed to determine why some cells are affected while others are not affected.

The maximum power of the module decreased by 6.2%. This is because only a few cells are shunted by the localized PID stress hence the effect on the entire module is small.

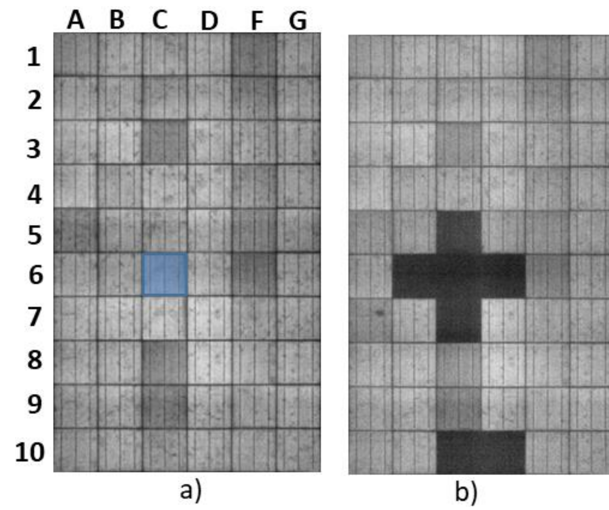


Fig. 5. Module C, EL images taken at 10% of Isc (0.982A), a) Initial EL image, b) EL image after 96 hours of PID stress.

5. Conclusion

PID was successfully induced by applying a sustained high voltage on a module using three methods as described. The presence of PID on the modules under test was detected from EL images taken at a current corresponding to 10% of Isc and from a measured decrease in maximum power after the applied PID stress. Cells affected by PID develop shunt current paths and appear darker in the EL image.

The results from method 3 show that PID was induced even on cells (C10 & D10) that were located far away from the cell (C6) where a local high voltage bias stress was applied on the module cover glass. This result indicate that the cover glass may be conductive at a high voltage and that certain cells in a module may be more prone to PID than others. This observation is being studied and will be reported in future.

Since methods 2 and 3 are done under artificial conditions, they may be useful in determining the PID susceptibility of the module at a particular point in time without subjecting it to

accelerated degradation as it may be in the case of Method 1.

Acknowledgements

The authors gratefully acknowledge the South African National Research Foundation (NRF), PVinsight (Pty) Ltd, National Laser Centre (NLC), African Laser Centre (ALC), the South African Department of Science and Technology (DST), ESKOM and Nelson Mandela University (NMU) for the financial support and providing necessary facilities for research.

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