Effects of varying the through silicon via liners thickness on their hoop stresses and deflections

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Abstract: Through silicon via (TSV) interconnect reliability is a problem in electronic packaging. The authors address the insertion losses, deflections which can result to separation of TSV layers and hoop stresses. These problems are due to different coefficient of thermal expansion between materials. The authors propose a robust methodology for (TSV) liners in this paper which in turn solves the reliability problem in (TSV). Silicon dioxide material is used in their paper as a TSV liner. First, they modelled the equivalent TSV circuit in advanced design systems (ADS). The authors then simulated it to obtain the TSV characterisation from which they obtained the S-parameter S21 which represents the insertion losses. Insertion losses have been described with changes in frequencies from 0 to 20 GHz with changes in TSV thickness from 7 to 8 µm. Later two different shapes of the TSV liner; the disc- and rod-shaped are modelled in analysis system 14 software. The two shapes with a radius of 5 µm each and a fixed pressure of 100 µPa developed changes in hoop stresses and deflections when the liners thicknesses are varied from 2 to 3 µm. The disc shape experienced least reliability problems so the authors propose its use in via structures.

1 Introduction

Moore's law [1] states that the use of high number of transistors are common in IC design. The expenses and technology challenges have been experienced with these approaches. To solve these problems, smaller transistors mounted on larger dies were implemented, although the entire problem was not solved. 3D technology has been thought to be the solution to all these problems although traditional 3D packaging technology is considered less beneficial when compared with the current (TSVs) technology. Due to this, TSVs have become widely used. However, there are problems which hinder its rapid development. Different materials have different coefficient of thermal expansion (CTE) which enhances this problem [2]. The incorporation of TSVs also poses a significant challenge to thermo-mechanical reliability of the 3D interconnects. Standards have been set for interposer size and pitch needed to meet performance standards. The international technology roadmap for semiconductors [3] projects TSV pitch remaining in the range of several microns, while on-chip interconnects pitch is in the range of 100 nm this is elaborated in Table 1.

1.1 Interconnect reliability problems

In 3D ICs, TSV noise coupling is one of the most significant consideration for circuit design [3, 4]. This is because the noise lowers the reliability of the via. Due to this, researchers have proposed the development of isolation between the via and silicon substrate. Electrical characteristics of TSVs, the resistance, capacitance and inductance determine the performance of 3D ICs. These are determined by configurations, geometrical dimensions and material properties of TSVs [5, 6]. TSV capacitance influences its electrical performance, latency, power loss and crosstalk [7, 8]. We modelled an equivalent TSV circuit with the electrical properties and then did the simulation to obtain the S21 parameter which defines the insertion loss. The TSV liner was made of silicon dioxide material. We varied the liner shapes, rod and disc together with the radius. Disc shape gave lower insertion loss compared with rod shape. Hoop stress and deflection were also simulated and disc shape still gave the least values. The time delay τ given by the product of resistance and capacitance increases with increase in capacitance [9]. Signal delivery in high-performance 3D integration systems requires the capacitance of each TSV lower than 100 fF [10]. TSV-TSV crosstalk, highly depends on the parasitic capacitances, liner capacitance and the substrate capacitance of TSVs [11, 12]. It also prefers low TSV parasitic capacitance for better signal integrity. In our model, we ensured least parasitic values for the integrity. This is evident in the results option.

1.1.1 Choice of materials: Silicon dioxide has been a commonly used via liner for ages now. It has several advantages for instance; native silicon dioxide is a high-quality electrical insulator and can be used as a barrier material during impurity implants or even diffusion. It can also be used for electrical isolation of semiconductor devices and also as a component in MOS transistors. Furthermore, silicon dioxide can be used as an interlayer dielectric in multilevel metallisation structures such as multichips. Silicon has become very dominant as a semiconductor material used in integrated circuits today because of its ability to easily form an oxide. However, some research work has been done on other materials which have some advantages not found in silicon dioxide or different forms of it. Research work [13] discussed that in the past several years, the inorganic dielectric $Si0_2$ formed by sol–gel process was studied extensively by the researchers [13, 14] as a potential substitution of the conventional thermally wet grown SiO_2 because of its technological interest. The technique was not only cheap and needed processing at high temperature for a shorter time but also only a small amount of raw materials was needed. Most importantly, the technique allows the use of multicomponent system. Researchers [3, 4] proposed a p^+ guard ring structure around signal TSV at different doping concentrations or levels. We also chose silicon dioxide as the material used around the TSVs due to its advantages but also came up with ways of reducing the reliability problems it experiences by using different shapes, varying the electrical characteristics and radius to reduce the insertion loss, deflections and hoop stress therefore increasing via reliability. Table 2 below gives its major properties which were essential in our modelling.

1.1.2 TSV shapes: We modelled rod and disc-shaped TSV liners. An ideal TSV is made up of some key areas such as the conductive

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Table 1 TSV and on-chip interconnects pitches

	2009	2012	2015
LeastOnInterconnects, nm	122	72	48
BonderOverlayAccuracy, m	1–1.5	1–1.5	0.2–1
LeastThicknessofStackedLayer, m	6–10	6–10	6–10
MostTSV AspectRatio	5:1–10:1	5:1–10:1	10:1–20:1
LeastPitchofTSV, m	2–4	2–4	1.6–3
LeastPitchforMonolithic3D, nm	90	64	44

pathway, the semiconductor, the dielectric, the bond pad and the land which acts as the ground [15]. The conductive pathway is normally made of copper which is a good conductor, therefore it constitutes a perfect interconnect. The dielectric material is the via liner which is normally made from silicon dioxide. The via liner offers protection to the via therefore reducing stress around it. The dielectric thickness can be varied to fit the producers' interest; hence, this raises the via reliability. The land is the ground through which the excessive charge flows while the bond pad interconnects either a chip or a via to each other. The TSV shape may or may not determine the TSV liner shape. It all depends on the manufacture interest.

Other researchers have defined rod and disc shapes in different ways. For instance, the authors [16] defined rod TSV as via with height-to-diameter ratios >2.5, while disc via has height-to-diameter ratios <0.25. He researched about the induced stresses in TSV and made a conclusion that there is an incentive for employing disc-TSV structures rather than rod structures. Suhir [17] stated that through-wafer copper vias especially their mechanical behaviour have attracted so much attention in the past [18–21]. The researcher [17] went further and explained that disc-like copper vias fabricated in silicon (Si) wafers often develop, due to the thermal expansion mismatch of the copper and the silicon materials at high temperatures, tensile stresses on the circumference of silicon. He described the situation to be intensified by the superposition of the stresses due to adjacent vias. He noted that when the vias are placed closer to one another and/or if the stresses in the Si wafer due to even a single via are high, either fatigue or brittle cracks might develop and grow through the wafer. However, the vias themselves would experience, at elevated temperatures, thermally induced compressive hoop stresses that could lead to the their buckling.

More work concerning via shapes and stresses have been done; it has been researched that the TSV can be classified into many categories such as via first or via last, via from top or via from back [22, 23]. TSVs with high aspect ratio in thick silicon on insulator with doped polysilicon filling were demonstrated. Some development of the Bosch etch process was necessary to achieve a good shape of the vias without voids. Depending on the integration strategy, the fill materials could include copper or wafer or polysilicon that may results in induced stresses in the silicon due to the CTE difference between the fill material and the silicon. Researchers [24] described the through silicon via (TSV) stress to be highly dependent on via shape, size and spacing. These three parameters place constraints on TSV design. They further summarised that in case trench via is fabricated, most of the stresses occur along the length of the via; however, shorter TSVs have less stress than longer TSVs, and the larger spacing between vias lowers stress experienced for a given length. Straight (rod-shaped) and tapered (V-shaped) TSVs [25] explained that rod-shaped TSV experience higher capacitance and conductance because of a larger surface area. Increased tapering reduces the area much more hence a much lower capacitance and conductance in the TSV at its lower surface.

Table 2 Physical properties silicon dioxide

Young's modulus, GPa	Poisson's ratio
66	0.17

2 Hoop stress theory and calculations

Researchers [26] defined hoop tension as the tangential component of stress which acts inside a collar at any radius due to the action of internal pressure. However, due to the absence of external pressure the value is assumed to be zero. The same experience applies to our model which has a double collar since it is whole therefore we use the same formula to calculate analytical hoop stresses experienced on our models. Hoop stress equation is given as

$$F_{\mathrm{h}} = wr_{\mathrm{i}}p_{\mathrm{i}} \quad (1)$$

where F_{h} is the hoop stress, w is the width of the collar, r_{i} is the internal radius, r_o is the external radius, p_{i} is the internal pressure and p_o is the external pressure. Substituting in (1) for each of the radius we used, we have

$$0.5 \times 7 \times 1000 = 3500\ \mu\mathrm{Pa} \quad (2)$$

$$0.5 \times 7.5 \times 1000 = 3750\ \mu\mathrm{Pa} \quad (3)$$

$$0.5 \times 8 \times 1000 = 4000\ \mu\mathrm{Pa} \quad (4)$$

Structural pressure has also been discussed [27]. Since our paper is not featuring optics, we did not pay more attention on this.

3 Methodology

First an equivalent TSV is modelled and simulated in advanced design systems (ADS) to give the S-parameter S21 which defines insertion loss which is a reliability problem. The electrical characteristics are well defined and the graph obtained behaved like an ideal via. Secondly, silicon dioxide is modelled at room temperature using ANSYS 14 software. Their radii from the centre of the via was varied as follows: 7, 7.5 and 8 μm considering a typical via size of 5 μm. The thickness of each via liner was 1 μm. This is done for both rod- and disc-shaped vias which are discussed in Section 1.1.2. After modelling, each via liner was exposed to an internal pressure of 100 μPa on their inner most layers and simulation done with each radii variation to obtain the hoop stresses and deflections. The results clearly showed that as the radii increased the values for the hoop stresses and the deflection decreased. Since stresses and deflections lower TSV reliability, we propose increase in the via liner thickness as a remedy to the problem. However, we realise that an increase in the thickness reflects to an increase in the chip size used. This is an expense. The power consumption also increased. To take care of these problems, we limited our simulation to a maximum via radius of 8 μm beyond which the problems percentages were a little higher. By doing so, our objective of lower hoop stresses and deflection was achieved hence increased via reliability.

4 Results

Fig. 1 shows an equivalent circuit of our TSV model. We paid less attention to the shapes but more on the electrical properties. The shapes are considered in Sections 4.1 and 4.2.

With the TSV in a horizontal position, Port 1 through to Port 2 represent the electrical components in the TSV which is made from copper. RTSV represents the resistance experienced along the TSV. We allocated them numbers 1, 2, 3 and 4 to differentiate them during simulation in ADS software. Inductance is also experienced along the TSV. They are also labelled 1, 2 and 3 to

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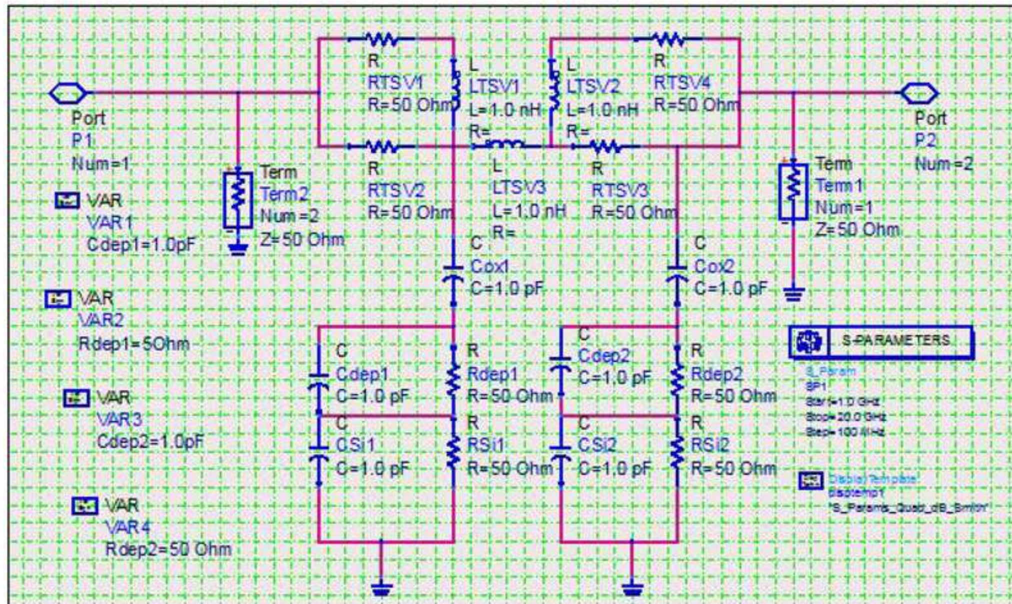

Fig. 1 *TSV equivalent circuit*

distinguish them. We included the terminations Terms 1 and 2 since they are requirements for S-parameter simulation. The results are shown in the next figure. Right after the TSV is the dielectric with acts as a liner offering protection to the via. In our case, we used silicondioxide material as a dielectric. Across the liner, capacitance was also developed. This is shown as Cox1 and Cox2.

We developed a depletion layer between the dielectric and the silicon substrate to prevent diffusion of dielectric into the substrate. Capacitance and resistances therefore developed. However, the capacitance and inductance vary, therefore the variable component VAR from the simulator. The numbers too represent each component. They are denoted by Cdep and Rdep. The numbers 1 and 2 just differentiate them. The last important part of the circuit is the substrate. It provided a surface whereby components were laid. However, it also experience capacitance and resistance. These contribute to reliability problem. The ground discharges excess charge.

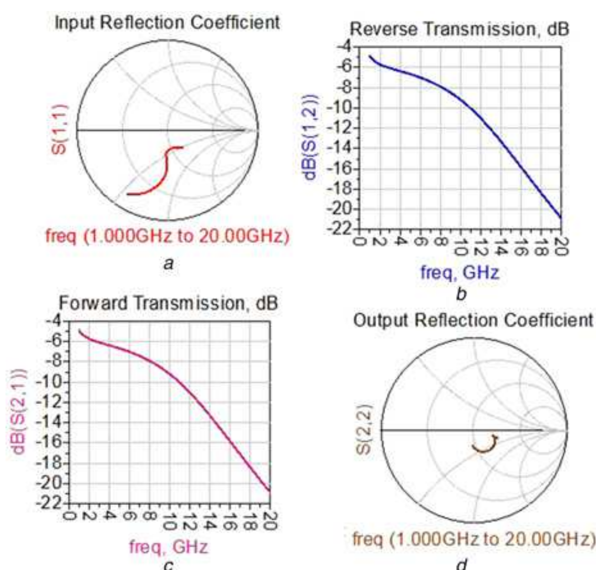

Fig. 2 *S-parameters*
a S11 – represents signal reflection which took place at port 1
b S12 – it shows the power transferred from port 2 to port 1. Since it's not equal to zero, not all power was delivered at port 1
c S21 – it shows the power transferred from port 1 to port 2. Since it's not equal to zero, not all power was delivered at port 2
d S22 – represents signal reflection which took place at port 2

Fig. 2 represents our simulation results from Fig. 1. Our focus went to Fig. 2*c* which gives the S21 parameter. It is concerned with insertion losses in TSV. This is a reliability problem which needed our attention. We divided the frequency into three main parts; between 0–2 GHz which we call A, 2–10 GHz which we call B and 10–20 GHz which is C. Various factors affected the insertion loss in these regions. In region A, insertion loss increased as the frequency increased due to decreased impedance of insulator capacitance. The overall insertion loss in regions A and B increased due to TSV diameter increase from 7 to 8 µm. Decrease in TSV inductance reduced the insertion loss in region C. In general, we reduced the insertion loss by increasing the silicon dioxide thickness from 7 to 8 µm. Since our model adhered to the ideal TSV electrical characterisation, we went ahead and modelled the rod and disc shapes separately using ANSYS software.

4.1 Rod-shaped TSV liner

The output looks like a rainbow because of the different colours; however, these colours have very important significance [28, 29].

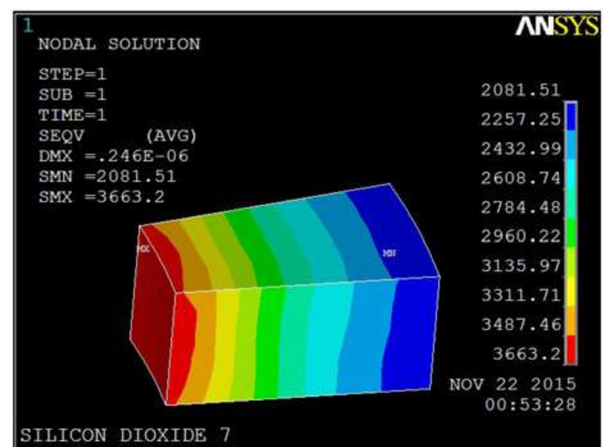

Fig. 3 *7 µm silicon dioxide rod*

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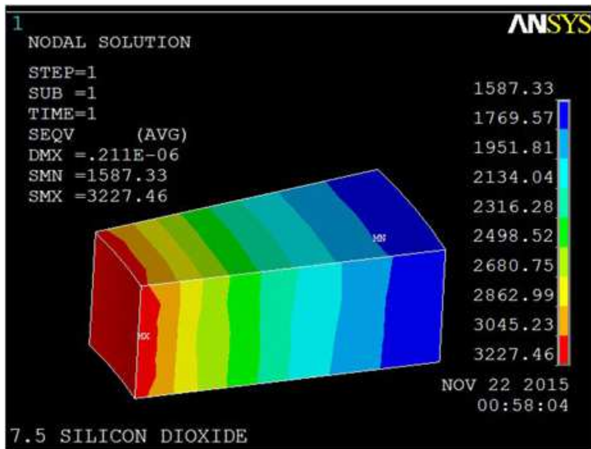

Fig. 4 *7.5 µm silicon dioxide rod*

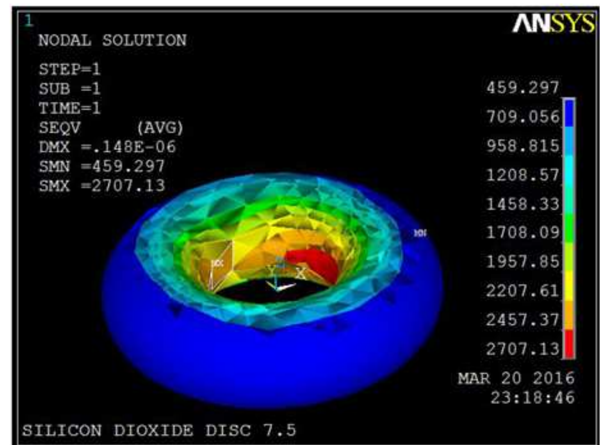

Fig. 7 *7.5 µm silicon dioxide disc*

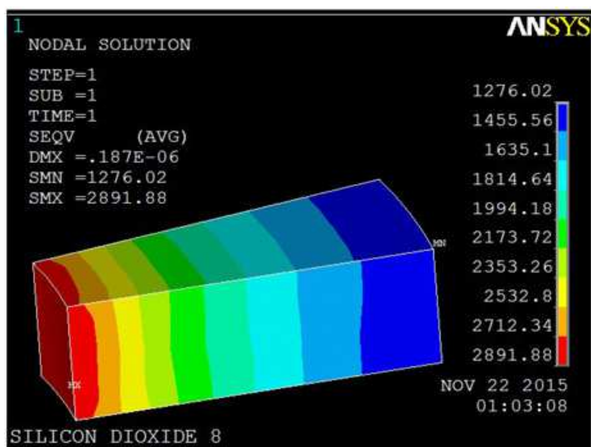

Fig. 5 *8 µm silicon dioxide rod*

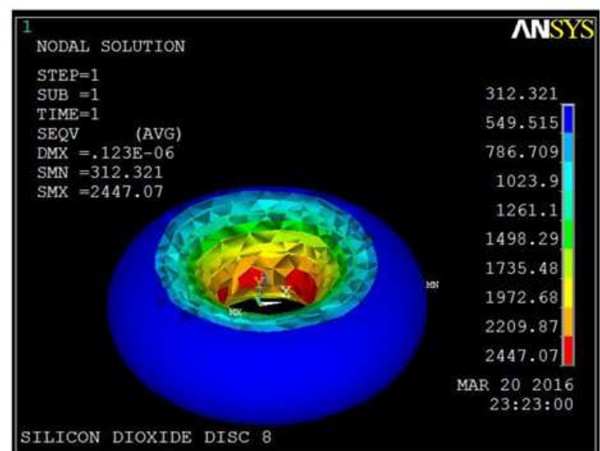

Fig. 8 *8 µm silicon dioxide disc*

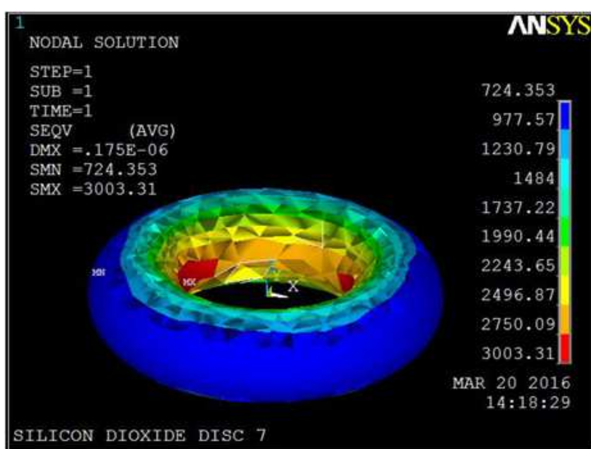

Fig. 6 *7 µm silicon dioxide disc*

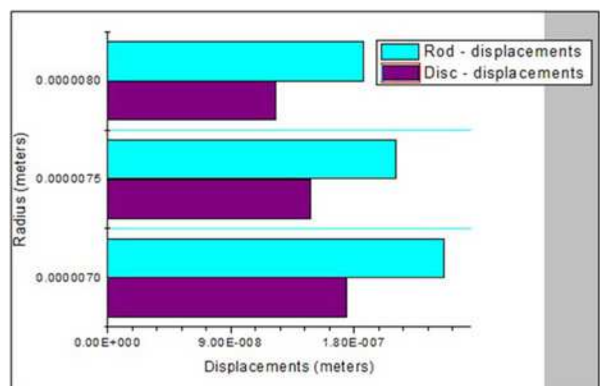

Fig. 9 *Displacements*

The red colour symbolises the highest level of stress, it is also considered as the hoop stress since its most impact will be felt on the circumference of the via liner; it is on this layer that the pressure was applied. The next layer is orange, then come green, light blue and finally deep blue. This is because the stress applied on the first layer keeps reducing therefore the region with the deep blue colour experiences the least stress (Figs. 3–5).

The vertical legend bar on the right side of each diagram gives the variations of stresses from the maximum to the minimum. On the left hand side are initials DMX representing the deflection which occurred, SMN representing the minimum stress value and SMX representing the maximum stress which is also the hoop stress.

4.2 Disc-shaped via liner

We referred to Figs. 6–8 as disc shaped since they have smooth edges unlike the rod one which appear sliced and with sharp

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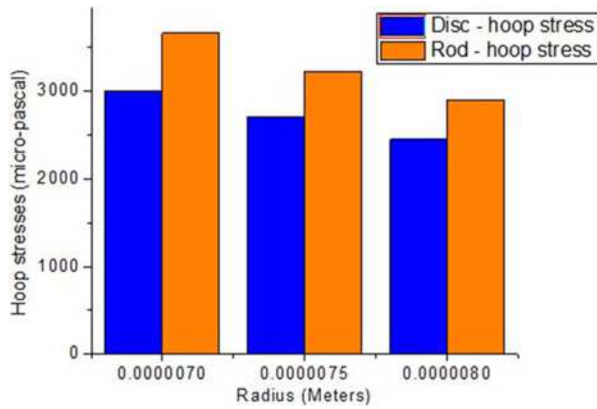

Fig. 10 *Hoop stresses*

edges. The vertical legend on the right side has the same meaning as those in rod shape. The same applies to the initials on the left side. Figs. 9 and 10 give a summary.

Fig. 9 shows variation of displacement with change in radii for both shapes. It is clear that as the radii increases, the value of deflection reduces. However, disc shapes developed lower deflections unlike the rod ones.

Fig. 10 is a plot of hoop stresses for both shapes. Disc shapes experienced lower hoop stresses than rod shapes.

A summary of hoop stresses and deflections in silicon dioxide TSV liner are shown in Tables 3 and 4, respectively. These values are also available on the respective vertical legends.

Table 3 clearly shows that as the radii of both rod- and disc-shaped TSV liners increases, the values of the hoop stresses decreases. However, the hoop stress values in rod-shaped liners were higher than those in disc shape. Since our objective is to achieve high reliability in the TSV liner, disc shape is better due to its lower stresses. The percentage differences are as follows

$$\frac{\mathrm{HS}_1 - \mathrm{HS}_2}{\mathrm{HS}_1} \times 100 = \mathrm{HSPD} \tag{5}$$

where HS_1 is hoop stress in the rod-shaped TSV liner, HS_2 is the hoop stress in the disc-shaped TSV liner and HSPD is the hoop stress percentage difference between rod- and disc-shaped TSV liners. Substituting the respective hoop stress values in each radii in (5) gives (6)–(8), respectively.

$$\frac{3663.20 - 3003.31}{3663.20} \times 100 = 18 \tag{6}$$

$$\frac{3227.46 - 2707.13}{3227.46} \times 100 = 16 \tag{7}$$

$$\frac{2891.88 - 2447.07}{2891.88} \times 100 = 15.38 \tag{8}$$

Equations (6)–(8) give the hoop stress percentage difference between rod- and disc-shaped silicon dioxide TSV liners at 7, 7.5 and 8 micrometre radius, respectively. The highest hoop stress

Table 3 Silicon dioxide rod- and disc-shaped TSV liners hoop stresses

Radius, μm	Rod-shaped hoop stress, μPa	Disc-shaped hoop stress, μPa
7	3663.20	3003.31
7.5	3227.46	2707.13
8	2891.88	2447.07

Table 4 Silicon dioxide rod- and disc-shaped TSV liners displacements

Radius, μm	Rod-shaped displacement, μm	Disc-shaped displacement, μm
7	0.246	0.175
7.5	0.211	0.148
8	0.187	0.123

percentage difference was experienced in the 7 μm radius TSV liner, the value being 18%. This shows that the disc shape has a higher reliability in the manufacture of TSV liners unlike the rod shape.

Table 4 on the other hand shows variations in displacements in both rod- and disc-shaped TSV liners with changes in radius. In both shapes, increase in radius decreases the displacements. We also noted that the displacements in rod shape were higher than those in disc shape. Due to reliability issue, we propose the use of disc-shaped TSV liner. The percentages are also as calculated as

$$\frac{\mathrm{DMX}_1 - \mathrm{DMX}_2}{\mathrm{DMX}_1} \times 100 = \mathrm{DMXPD} \tag{9}$$

where DMX_1 is the displacement in rod-shaped TSV liner, DMX_2 is the displacement in disc-shaped TSV liner and DMXPD is the displacement percentage difference between the two shapes in either rod- or disc-shaped TSVs. Substituting the values of displacements at each radii in (9) yield

$$\frac{0.246 - 0.175}{0.246} \times 100 = 28.86 \tag{10}$$

$$\frac{0.211 - 0.148}{0.211} \times 100 = 29.86 \tag{11}$$

$$\frac{0.187 - 0.123}{0.187} \times 100 = 34.22 \tag{12}$$

Equations (10)–(12) give the displacements percentage difference between rod- and disc-shaped silicon dioxide TSV liners at 7, 7.5 and 8 micrometer radius, respectively. Here, the highest percentage displacement was experienced in the 8 μm radius TSV liner which was 34.22%. Therefore disc-shaped TSV liner experienced a lower displacement therefore we recommend it in the manufacture of TSV liners since it will promote via reliability.

5 Discussions

In our research, we experienced the same problems. Due to the increase in the thickness of the TSV liner, this translated to an increase in the size of chip used. A bigger chip meant that more power was used in our work. Apart from the power, the cost of the bigger chip meant more expenses to us. The distance between one TSV and another also increased so a longer interconnect needed and this slowed down the signal speed. Considering the dimensions we chose for our TSV liners, the effects were very minimal compared with the interconnect problem we were solving, so we ignored them. We were able to lower the insertion losses, hoop stresses and deflections experienced around the TSV liners therefore increasing the TSV reliability. It is also clear as per our paper that the disc shape TSV liner gave lower values than the rod shaped. Although the values were low, the insertion losses, hoop stresses and deflections were not too little or zero. This means that they still exist and have not been completely eradicated. This is still a reliability problem and more works should be done to reduce the values to the minimum or if possible zero.

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6 Conclusion

ADS was used to find the insertion loss in TSV. The graph behaved like an ideal TSV hence this gave way to the next modelling where the effects of changes in TSV liner thickness on the experienced hoop stresses and deflections was also done. When exposed to pressure on their inner most layers, the hoop stresses and deflections decreased in value with increase in their thicknesses. Since reliability in interconnects is highly affected by high stress, increased TSV liner thickness can be used to solve that problem. However, the shape and material also determines the level of hoop stress and deflection experienced. Hoop stress and deflection values were least in disc-shaped TSV liner unlike the rod-shaped one. Disc-shaped silicon dioxide TSV liner reduced the hoop stress experienced at most by 18% and deflection at most by 34.22%. We therefore recommend disc-shaped silicon dioxide TSV liner in the manufacture of TSV liners. However, more work can still be done on TSV liners unlike the TSV themselves to eradicate the reliability problems in TSV completely. We observed that more work has been done on TSV unlike the TSV liner which offers its protection.

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