Abstract

Through Silicon Via Interconnects are usually protected with liners. A research on liners was done and conclusion made that they experience reliability problems like hoop stress which put them and the Through Silicon Via in danger. Simulation using Analysis Software was done on Silicon Dioxide liner. A Through Silicon Via of internal radius five micrometers, silicon liner of thickness two micrometers and height one micrometer was used. The liner was subjected to an internal pressure of one thousand micro Pascal. From mechanical Analysis System Parametric Design Language fourteen, it was confirmed that hoop stress surely exists in liners and ways should be proposed to protect them alongside the Through Silicon Via.